Total Ionizing Dose (TID) and Displacement Damage (DD) Effects in Integrated Circuits: Recent Results and the Implications for Emerging Technology

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Abstract

Over the last 50 years, the effects of cumulative radiation damage in microelectronics, and now nanoelectronics, have continually presented a design and assurance challenge to space flight missions. Feature sizes, that is, the size of the unit structure in microelectronics, has continually decreased, which has presented an added complexity to testing and assuring microelectronic devices. This paper outlines the paradigm shifts of total ionizing dose (TID) and displacement damage (DD) effects as device sizes have reduced and highlights some of the strategies developed to insert apply microelectronics into space. The current trends of the technology are analyzed in context of future JPL and NASA missions.

1. Introduction

With the recent deployment of the Mars Science Lander and Juno missions, the Jet Propulsion Laboratory (JPL) reaffirmed a long history of launching spacecraft to remote and harsh locales of the solar system. Of course the space radiation environment presents a unique assurance challenge to all spacecraft designs. The Juno mission, also called the Jupiter Polar Orbiter, will travel through the radiation belts of Jupiter and endure a severe radiation environment [1]. Such mission profiles to the moons of Jupiter or orbits toward the Sun, like Goddard Space Flight Center’s Living with a Star (LWS) program are presenting ever-increasing requirements on radiation assurance. Total ionizing dose (TID) levels over 300 krad(Si) are expected for any mission to a Jovian moon [2], [3]. To enhance mission capabilities, the use of advanced technologies is in demand. However, it adds a layer of complexity when assuring the survivability of those devices in such environments.

2. CMOS radiation effects

2.1 Historical Trends in Radiation Effect as Devices Scale Down

The trend of scaling and increased performance due to reduction in feature size has been governed by and large by Moore’s law [4]. Moore’s law has stated that in microelectronic devices, especially in CPUs,
transistor count doubles and the feature size reduces by 30% every 2 years. Twenty two nanometers gate length is the current feature size in modern devices. This feature size and the design rules that follow determine the density of memories, which is critical to the space science and communication community as the data and bandwidth needs have driven the need for highly scaled memories and data processors for space missions.

Fig. 3. Side-wall leakage path in a STI structure. The interface between silicon and silicon dioxide always presents a perspective leakage path.

Fig. 4. Inversion measurements for 180 nm test structures irradiated under different bias conditions.

The main effect of TID on microelectronics is the effect liberated charge has on the insulating silicon dioxide (SiO₂). Fig. 1 shows the typical response of trapped charge in the oxide of an N-channel metal oxide silicon (MOS) structure. The polarity of the charge liberated in an oxide is trapped according to the nature of the local silicon. In an N-channel device, the charged trapped at the interface is negative, that is, electrons, and the bulk oxide that is away from the interface, is holes. The relative trapping rate of charge in the interface versus the bulk determines the overall response of the devices. All N-channel devices, if irradiated long enough, will show the behavior in Fig. 1. The dose level at which one type of charge out numbers another depends on many factors, such as dose rate, gate bias, oxide thickness and temperature. A P-channel device, on the other hand, will have only trapped holes, so the effect is a solely negative threshold shift on the MOS structure. As the gate oxides of advanced CMOS technologies scale to thinner dimensions, the threat of shifts in DC parameters due to oxide trapped charge (N_{ox}) buildup in the gate oxide is reduced as shown in Fig. 2.

These results would indicate that as features size reduces, the TID hardness of a device will increase. If only the gate oxide is considered, then one could expect that TID effects will disappear [5]. Instead, as devices shrink, radiation-induced charge buildup in field oxides has become to dominate the degradation and induces leakage currents. Indeed, the structure of a highly scaled modern device consists of several isolation oxide structures with thicknesses (~300 nm) order of magnitude higher than the gate oxide. The field oxide is more prone to traps that, when charged, present a voltage shift to the channel or surrounding silicon [6]. This results in MOSFET threshold shifts or a parasitic leakage path through the local silicon. Processing changes like shallow trench isolation (STI) or devices constructed on silicon on insulator (SOI)
processes have been proposed to reduce these effects, but STI suffers from side-wall leakage paths and SOI suffers from back channel leakage [7].

2.2 Radiation Effect is Advanced MOS Structures and Devices

Recent studies at JPL have addressed many of these issues for TID. JPL’s goal for a Jovian moon mission would be 1 Mrad(Si) hard microelectronic devices, and even after one inch of aluminum shielding the expected dose level is 300 krad(Si). So considerable thoughts at JPL have been expended to develop strategies to assure proper device operations to these dose levels. Johnston et al. have done considerable work in recent years about the radiation hardness of CMOS structures. For example, Fig. 3 shows the simplified STI structure along with the suspected drain-to-source parasitic leakage path possible if the STI oxide traps enough charge [8]. The effect is modulated by the distance of the oxide from the channel of the MOSFET and the length of the parasitic path, which implies that the proper architecture for a CMOS device can vastly mitigate field oxide or STI leakage. The irradiation bias is an ever present problem for CMOS as Fig. 4 shows. The same structure as Fig. 3 is shown modeled to a 180 nm process and the damage is noticeably worse at higher bias, which is an inescapable fact of CMOS TID effects.

The driving requirement for more bandwidth and data depth in space missions, especially for JPL, has driven the use of commercial off the shelf (COTS) solutions. Among other, memories with high capacity are in demand and for instance, the only current high density non-volatile memory (NVM) option is the floating gate based flash memory. Both NAND and NOR based flash memories are used and are heavily tested to find uniquely robust devices. Densities of flash memories are currently at 32 Gbit and multiple bits of information can now be stored on a single cell. The erasure of a flash device by TID has been known for some time; however, the primary TID failure mechanism of flash memory currently lies in the charge pump of the device. Fig. 5 shows the number of errors in a multi-level cell (MCL) NAND flash due to the degradation of the charge pump [9]. Bagatin et al. showed for modern flash memories the output of the charge pump drops immediately with dose and eventually cannot support programming or erasing the device around 50 krad(Si) [10]. A similar response was seen for NOR flash in Fig. 6 where the errors grow exponentially with doses [11]. Both NAND and NOR flash memories exhibit 100% error coverage around 50 krad(Si) and is considered to coincide with the charge pump failure. The support circuitry for flash memory, however, has seen the benefits from the decrease in feature size, so the effects of TID on the leakage paths of the control circuitry has been seen to decrease for more dense devices as shown in Fig. 7 [12]. Since memory retention TID effects and charge pump degradation can be mitigation, the TID effects on control circuitry with remain an issue for flash memory.

![Fig. 7. Standby current results versus dose for Micron Technology 1, 2 and 4 Gb SLC NAND flash memory in No Refresh Mode.](image)

![Fig. 8. Charge trapping effect in a PNP bipolar transistor. The reduction in gain due the increase recombination causes bipolar device failure.](image)

![Fig. 9. Atomic iteration of a particle in a depletion region. This is the core interaction of DDD damage.](image)

![Fig. 10. DDD accrual in the transistor region of a PNP device.](image)
3. Bipolar Radiation Effects

3.1 Radiation Effect in Modern Bipolar Devices

Bipolar devices, unlike CMOS, have evolved toward greater precision and efficiency in recent years. This is mainly because bipolar technologies are predominantly used in measurement and telemetry applications, which by and large do not require a significant density to function in a space system. Bipolar ICs that have been designed in the context of Moore’s law have received some of the benefit in modern devices; however, the effects of these are seen in the size or density of newer devices. At the core of dose effects on bipolar ICs is the effect of radiation on the bipolar junction transistor (BJT). Fig. 8 shows how the oxide that exists near the transistor region of the device is affected by TID. The trapped charge in the oxide increases the recombination in the base-emitter region by influencing the depletion region of the device. The result of this increase in recombination is a decrease in the gain of the transistor. Both PNP and NPN have a similar drop in gain, but the magnitude of the drop depends on the irradiation conditions and architecture of the device. Recombination of the bipolar device will also increase if the minority carrier lifetime decreases. Atomic dislocations from irradiation, called displacement damage (DD or DDD for displacement damage dose), reduce minority carrier lifetime as shown in Fig. 9. Fig. 10 shows how the displacement damage in a bipolar transistor reduces the gain. In both cases of TID and DDD irradiation, the damage to the bipolar transistor, which is the primary constituent device of a bipolar IC, will affect any parameter of the IC that depends on the integrity of the transistor. As the parameters of the constituent device on a bipolar IC degrade, the performance of the device will degrade. Matched transistors in an operational amplifier will induce more offset voltage as the damage increases. Finally, as the forced gain requirements of the device are not met, the device will exhibit functional failure.

Bipolar devices are unique in TID sensitive devices in that the rate at which the bipolar IC is irradiated affects the magnitude of the damage. The effect has been named Enhanced Low Dose Rate Sensitivity (ELDRS) but should be noted that since it is seen to occur that dose rates over 0.01 rad(Si)/s or 300 krad(Si)/year, it is actually more of an artifact of the laboratory high dose rate testing. It this vein ELDRS should be called Reduced High Dose Rate Sensitivity. The ELDRS basic process is due to the self-interaction of injected charge in the oxide near the passivation layer that reduces trapping by increasing recombination and charge transport. Fig. 9 presents the archetypical ELDRS response in a bipolar device. Many bipolar ICs have saturated ELDRS response at 0.01 rad(Si)/s, but as Fig. 9 shows, some devices show continued ELDRS response at lower dose rates.

![Fig. 9. ELDRS effect in JFET input stage OPAMP.](image1)

![Fig. 10. Enhancement of the ELDRS effect as a function of hydrogen.](image2)
3.2 Recent Bipolar IC Radiation Test Results

The lion’s share of recent research at JPL into the ELDRS has focused on understanding the dynamics of the effect. The presence of hydrogen in or near the passivation layer of the device was postulated to aggravate the effect. Taken from [15], Fig. 10 shows the effect of hydrogen concentration in a device. The amount of hydrogen does two things: 1) it increases the degradation at LDR; i.e. the saturated ELDRS effect by a factor of up to 10; 2) it increases the dose rates region where the transition from high dose rate (HDR) to low dose rate (LDR) enhancement occurs. Fig. 11 shows the continuation of the research for various dose rates and hydrogen concentrations [16]. The presence of hydrogen near the passivation results in more ionic hydrogen attaching to dangling bonds at the passivation/oxide interface and this condition results in more trapping sites. It is important to note that the ELDRS effect is present even when the hydrogen concentration is zero.

Other EDLRS studies sought to understand the nature of charge migration in irradiated bipolar devices. Fig. 12 shows the effect of irradiating a bipolar device at various temperatures to study the charge transport effects [17]. The lower temperature irradiations resulted in less measured shift. The results were correlated to a continuous random walk (CTRW) model to explain the observed ELDRS effect.
Since the target goals of various JPL missions reflect TID levels between 300 and 1000 krad(Si), the effects of these dose levels at LDR is of great interest. Since the difference between HDR and LDR will affect results in each constituent device of the IC differently, the overall response of a complex bipolar IC to LDR at high dose levels is hard to predict. Recent testing at JPL has shown this to be true [18]. Fig. 13 and Fig. 14 show LDR tests to 1 Mrad(Si) for two COTS devices. As expected the LDR in the unbiased condition is the worst case, however the effect saturated and seem to rebound in the case shown in Fig 13. This effect was postulated to be due to the competing degradation of devices in the IC. In both cases, the LDR biased condition was the least responsive. Both of these cases show the HDR testing was not able to predict the final LDR response. HDR testing was also not able to predict device failure, as seen in Fig. 15, where the LDR testing of a device resulted in functional failure not seen in the HDR testing. Finally, Fig. 16 shows the inevitable functional failure of a voltage regulator at high enough dose in LDR testing.

4. Conclusion

CMOS technology has continually increased in capability and density. And in these changes, TID effects have evolved with the device. Gate leakage and shifts have been replaced by similar effects due to side-wall leakage in STI, back channel leakage in SOI and side-channel leakage for field oxides. These effects however have been able to be addressed in many rad-hard designs. The primary limit to CMOS and bipolar ICs is the underlying silicon. Silicon is at its efficiency and bandwidth limit, and therefore presents a mass, speed and power limitation to both very large and very small JPL missions. Some exotic silicon structures like FINFET or FOXFET allow for devices to advance, but the fundamental limits are the same. Proposed technologies like graphene based ICs offer much lower power for the same speed allowing for very small space missions, which allow for unprecedented mission flexibility. Alternate device materials, like SiC or GaN, offer speed and power options to space applications.

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B. References


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