A Voltage and Temperature Stable Threshold-Voltage Reference Circuit

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Summary

An improved threshold-voltage reference (V_{TR}) circuit operated at subthreshold current region has been presented and compared with a bandgap-voltage reference (V_{BR}) circuit. MOSFET threshold voltage as reference source makes it possible to control output voltage V_{TR} by substrate bias. Since drain voltage difference affects I-V characteristics even in subthreshold region, drain voltage equalization by adding an n-MOSFET improves voltage- and temperature-dependence of the V_{BR}/V_{TR} circuits. The circuits were fabricated by 1.2 μm n-well CMOS process. $V_{BR}\approx1.26$ V and $V_{TR}\approx1.29$ V were obtained for both circuits. The change of (V_{BR}/V_{TR}) for the supply voltage $V_{DD}=5.0\pm1.0$ V and T=−60～+100°C was improved from (3.3/2.8) to (1.1/1.0) %. V_{TR} reference had a little larger fluctuation of output voltage at $V_{DD}=5.0$ V and T=+20°C, but a little smaller V_{DD} and T dependence. V_{TR} was controlled from 1.29 to 1.71 V by the substrate bias voltage V_{Sub} supplied to n-MOSFETs from 0.0 to −2.0 V, and the change of V_{TR} for $V_{DD}=5.0\pm1.0$ V and T=−60～+100°C was further improved from 1.0 to 0.6 % by V_{Sub} supply.

Key words: threshold-voltage reference, bandgap-voltage reference, CMOS

1. Introduction

Combined analog-digital CMOS LSIs are becoming attractive as the integrated systems become larger and complex. The needs for the voltage- and temperature-stable voltage reference become important for the analog LSIs, because, for an example, the absolute accuracy of data conversion system is limited by the accuracy of the voltage reference. Recently, the reference voltage generator has been integrated in the battery operated memory chips. The integrated low-voltage references become necessary as the supply voltage gets lower due to the MOS device scaling down as well as the battery operated LSI systems are popular.

Concerning MOS LSIs, voltage references that use the gate work-function difference [1] and the threshold voltage difference between enhancement/depletion n-MOSFETs [2], [3], which was recently improved by using dynamic operation to reduce power consumption [4], were reported. On the other hand, the bandgap voltage reference using bipolar transistors [5], [6] has been widely used in bipolar LSIs, and becomes a standard technology. Many studies have been proposed to apply this bipolar technology to CMOS process. The basic idea is based on the use of n-MOSFETs under bipolar-like subthreshold current characteristics in weak inversion instead of the bipolar transistors [7], the combination of the CMOS compatible vertical bipolar substrate-transistor and n-MOSFETs operating in weak inversion [8], [9], the combination of the CMOS bandgap reference circuit and op-amp [10, 11], and the use of CMOS compatible lateral bipolar transistors with small gate length [12], [13]. The above mentioned bandgap reference voltages are nearly fixed around Si energy bandgap of 1.2 V [8]-[13], which limits a low supply-voltage operation below 1 V. Recently, an improved CMOS bandgap reference circuit with sub-1-V operation was proposed, which composed diodes of substrate-bipolar-transistors, resistors and a CMOS op-amp fabricated by n-well CMOS process[14]. Its reference voltage can be freely lowered from the conventional bandgap reference voltage by controlling the resistance ratio of the circuit.

This paper describes a voltage- and temperature-stable MOSFET's threshold-voltage reference (V_{TR}) circuit using resistors, n-MOSFETs biased in subthreshold current region, and an n-MOSFET to generate the threshold-voltage

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reference, which is used instead of a bipolar transistor to generate the bandgap-voltage reference [15], [16]. The supply voltage and temperature dependence of the V_{TR} circuit is compared with the same circuit using a diode to generate the bandgap-voltage reference (V_{BR}). Though the V_{TR} depends on the fluctuation of the threshold-voltage V_T, the circuit makes possible a low power operation as well as fully compatibility with CMOS technology independent of its well type. Furthermore, its reference voltage can be controlled down to the extrapolated threshold voltage to 0 K, which is sufficiently below 1 V applicable to the future low voltage supply.

2. Bandgap-Voltage Reference and Threshold -Voltage Reference

Figure 1 shows a bandgap-voltage and a threshold-voltage reference circuit using a diode D3 or an n-MOSFET N3 as a reference-voltage generating device, respectively. The subthreshold current I_S of the MOSFET in the weak-inversion mode is given by

$$I_S = I_s \exp[(V_{GS} - V_T)/nV_t] \quad (1)$$

where I_s; the temperature independent I_S current, V_T; the threshold voltage, n; the fitting factor for MOSFET's subthreshold swing and V_t; the thermal voltage (=kT/q). The diode current I_D is given by

$$I_D = I_d \exp[(V_D - E_g)/V_t] \quad (V_D \geq 3V_t) \quad (2)$$

where I_d; the temperature independent I_D current and E_g; the energy bandgap of Si. The temperature independent I_s, I_d and n are assumed to simplify the discussion below. Furthermore, the substrate bias effects on I_S of N2 n-MOSFET is neglected. Currents I_{S1}, I_{S2} and I_D are given as

$$I_{S1} = I_{s1} \exp[(V_{GS1} - V_T)/nV_t] \quad (3)$$

$$I_{S2} = I_{s2} \exp[(V_{GS2} - V_T)/nV_t]$$

where $V_{GS2} = V_{GS1} - R_1 I_{S2}$ (4)

$$I_D = I_d \exp[(V_D - E_g)/V_t] \quad (5)$$

We assumed that p-MOSFETs P1/P2/P3, which compose the current-mirror circuit, have the same geometry, then $I_{S1}=I_{S2}=I_D$ is satisfied. The bandgap-voltage reference V_{BR} is given by

$$V_{BR} = V_D + R_2 I_D = V_D + V_t(nR_2/R_1)\ln(I_{s2}/I_{s1}) \quad (6)$$

Assuming that R_1 and R_2 have the same temperature coefficient and V_D is biased to keep the I_D current constant, the temperature coefficient of V_D is

$$\partial V_D/\partial T = -[E_g(T) - (\partial E_g/\partial T)T - V_D]/T$$

$$= -(E_{g0} - V_D)/T \quad (7)$$

where E_{g0} is the energy bandgap at T=0 K.

To realize $\partial V_{BR}/\partial T = 0$, the (R_2/R_1) ratio must satisfy

$$R_2/R_1 = (E_{g0} - V_D)/nV_t \ln(I_{s2}/I_{s1}) \quad (8)$$

The (I_{s2}/I_{s1}) ratio is proportional to the (W_2/W_1) ratio (i.e,. the channel width ratio of N1 and N2 n-MOSFETs, while the same channel length L is assumed). Substituting Eq. (8) into (6), then

$$V_{BR} = E_{g0} \approx 1.21 \text{ V} \quad (9)$$

because $E_g(T) = E_{g0} + (\partial E_g/\partial T)T = 1.206 - 2.73 \times 10^{-4} T$ (for $T \geq 250$ K) [17]. Eq. (9) means that the temperature stable voltage reference V_{BR} is realized around the bandgap voltage at T=0 K ; $E_{g0} \approx 1.21$ V (i.e., the bandgap-voltage reference). Consequently, the bandgap-voltage reference is precisely stabilized from the temperature variation by controlling I_S and V_T matching, (W_2/W_1) ratio, (R_2/R_1) ratio and the temperature coefficient matching of R_1 and R_2. The above four conditions are easily satisfied for the modern MOSFET process, and the bandgap-voltage reference method has been widely used to

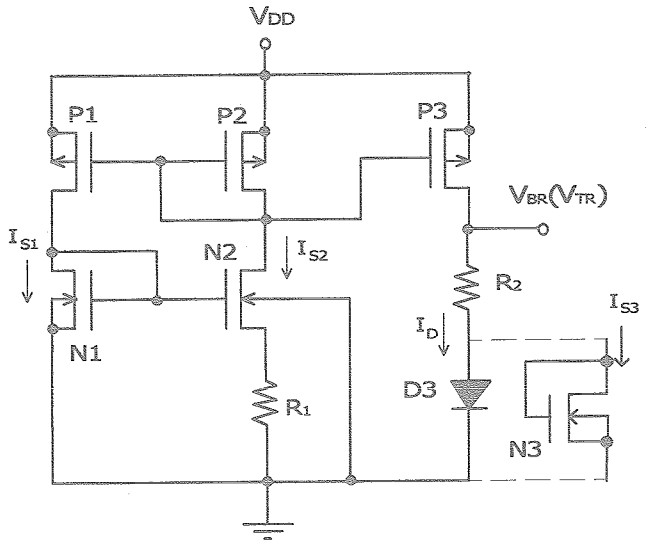


Fig. 1. A bandgap-voltage reference (V_{BR}) circuit using a p-n diode D3, and a threshold-voltagereference (V_{TR}) circuit using an n-MOSFET N3.

generate the standard voltage reference. However, the stabilized voltage V_{BR} is limited around E_{g0} due to its theoretical background. When the target V_{BR} is lower than E_{g0}, V_{BR} should be down converted.

Concerning the threshold-voltage reference, I_D of Eq. (5) is replaced by

$$I_{S3}=I_{s3}\exp[(V_{GS3}-V_T)/nV_t] \quad (10)$$

The threshold-voltage reference V_{TR} is given same as Eq. (6),

$$V_{TR}=V_{GS3}+R_2I_{S3}=V_{GS3}+V_t(nR_2/R_1)\ln(I_{s2}/I_{s1}) \quad (11)$$

When V_{GS3} is biased to keep I_{S3} constant, the temperature coefficient of V_{GS3} is given similar to Eq. (7),

$$\partial V_{GS3}/\partial T=-(V_{T0}-V_{GS3})/T \quad (12)$$

where V_{T0} is the threshold-voltage at temperature T=0 K. To realize $\partial V_{TR}/\partial T=0$, the (R_2/R_1) ratio should satisfy

$$R_2/R_1=(V_{T0}-V_{GS3})/nV_t\ln(I_{s2}/I_{s1}) \quad (13)$$

Substituting (13) into (11), V_{TR} is given by

$$V_{TR}=V_{T0} \quad (14)$$

and thus V_{TR} is a temperature stable threshold-voltage reference around V_{T0}.

The features of V_{TR} voltage reference in comparison with V_{BR} voltage reference are as follows; (1) simple process and full compatibility with CMOS process and device, and (2) scalability of V_{TR} voltage, which can correspond to the future trend of supply voltage V_{DD} lowering. V_T becomes lower as V_{DD} becomes lower, and thus V_{TR} can follow the V_{DD} lowering. However, V_{BR} is limited around 1.2 V because of the physical constant E_{g0}. When V_{TR} voltage is too small for the target voltage, it can be converted to a higher voltage by using a standard amplifier technique. According to Ref. [18], minimum analog supply voltage becomes 1.8~1.5 V around 2008. Consequently, V_{BR} voltage reference reaches to its limit near future. On the contrary, the demerit of V_{TR} voltage reference is the larger fluctuation of V_{T0} in comparison with physical constant of E_{g0}, which means the difficulty of precise V_{TR} control. However, 3σ variation of V_T less than 40 mV even in the minimum L device for digital use will be realized over 2004 as described in Ref. [18]. Those values are much smaller for long L device, and V_{T0} variance will become smaller as the technology advancements.

3. Experimental Results and Discussion

Figure 2 shows the revised V_{BR}/V_{TR} voltage reference circuit. A cascode device of N4 n-MOSFET between P5 p-MOSFET and N2 n-MOSFET is added to the basic V_{BR} circuit given in Fig. 1 [15], [16]. The gate of N4 is connected to the (drain/gate) of N8. The drain voltage difference between N1 and N2 causes a mismatch of current mirror even under subthreshold current region. N4 equalizes the drain voltages of N1 and N2 resulting in keeping the theoretical condition of $I_{S1}=I_{S2}$ strictly, and can effectively improve both V_{DD} and T dependence as discussed in Figs. 5 and 6. The start-up circuit is also added for a stable operation. The circuits were fabricated by 1.2 μm n-well CMOS process. The channel length L of all n-MOSFETs is 1.85 μm. The channel width W and L of all p-MOSFETs are the same in the two-stage current-mirror circuit, which is used to obtain superior stabilized V_{BR} or V_{TR} characteristics against V_{DD} and T. The (W_2/W_1) ratio is 8. The R_1 and R_2 resistors are the n-well resistors and R_1 is about 50 kΩ. The D3 p-MOSFET fabricated in the n-well is used as a forward-biased p-n diode to generate V_{BR} voltage. N3 n-MOSFET is used to generate V_{TR} voltage.

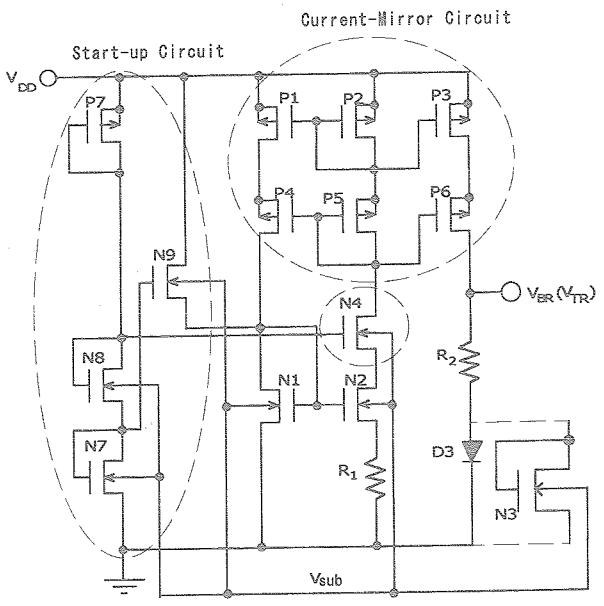


Fig. 2 The revised V_{BR}/V_{TR} voltage reference circuit. The two-stage current-mirror circuit is used. The start-up circuit and N4 n-MOSFET are added to the original circuit given in Fig. 1.

Figure 3 shows photomicrographs of (a) main V_{BR}/V_{TR} voltage reference circuit, and (b) R_1/R_2 resistors. R_1 is fixed at around 50 k Ω , while R_2 can be controlled by changing the connection from 100 to 840 kΩ by 1.25 kΩ (i.e., R_2/R_1 ratio ranges from 2.0 to 16.8 by 0.025 step). Optimum (R_2/R_1) ratio to minimize V_{BR}/V_{TR} variation dependent on V_{DD} and T can be easily controlled.

At first, E_{g0} and V_{T0} given in Eqs. (9) and (14) were measured for D3 p-MOSFET and N3 n-MOSFET as shown in Fig. 4. Figure 4(a) gives temperature dependent I_S versus (V_G=V_D) characteristics of N3 n-MOSFET. The measured temperatures T were at −60, −20, +20, +60 +100°C. The similar I_D characteristics were also measured for D3 p-MOSFET. Figure 4(b) gives V_D or V_{GS} versus T characteristics for various constant I_D and I_S current levels. V_D and V_{GS} values extrapolated to T=0 K give E_{g0}=1.21 V and V_{T0}=1.21 V, respectively, independent of I_D and I_S currents. The same 1.21 V for both E_{g0} and V_{T0} is accidental for this chip, because V_{T0} should depend on the fabrication conditions.

An example of temperature dependence for V_{BR} and V_{TR} at V_{DD}=3, 4, 5, 6 and 7 V under the best (R_2/R_1) ratio are given in Figs. 5 and 6, respectively. (a) and (b) of Figs. 5 and 6 show the difference of V_{BR}/V_{TR} data without N4 and with N4 n-MOSFET, respectively, to demonstrate the effectiveness of N4 device. At the typical condition (i.e., V_{DD}=5.0 V, T=+20°C),

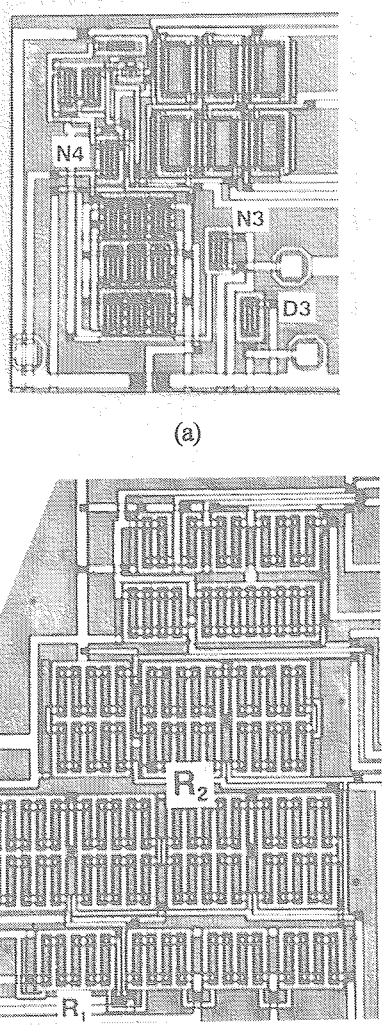
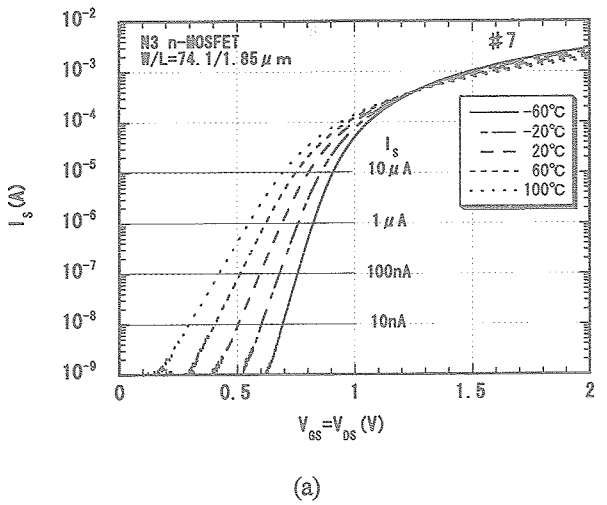


Fig. 3. Photomicrographs of V_{BR}/V_{TR} voltage reference circuit. (a) Main circuit and (b) R_1/R_2 resistors.



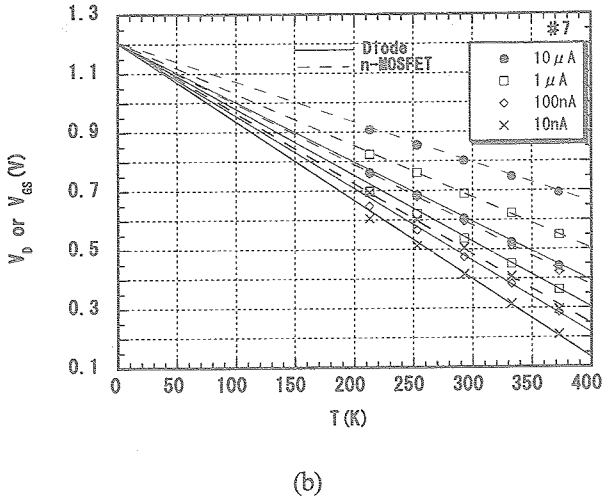
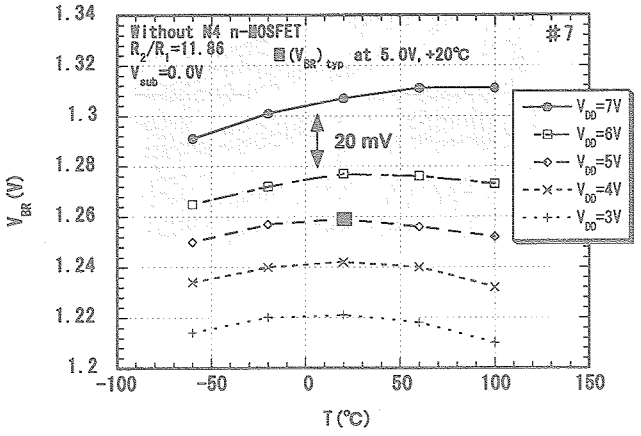
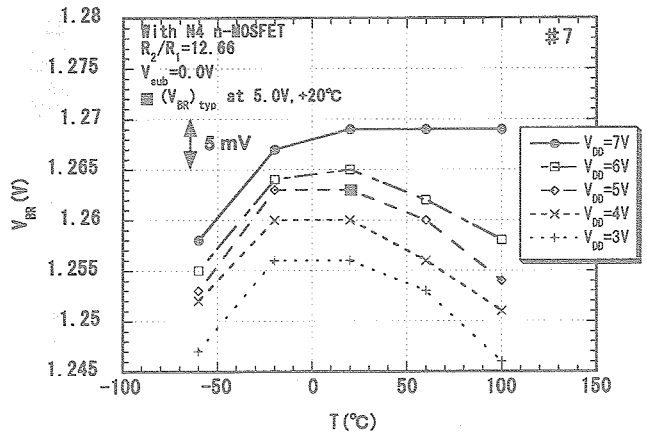


Fig. 4. (a) I_S versus (V_{GS}=V_{DS}) curves of N3 n-MOSFET for generating V_{TR} reference. (b) E_{g0} and V_{T0} obtained by extrapolating the measured data to T=0 K at various constant I_S and I_D current levels.

$(V_{BR})_{typ}$=1.259/1.263V and $(V_{TR})_{typ}$= 1.297/1.294 V were measured for without/with N4 n-MOSFET at the supply current of about 6 μ A. $(V_{BR})_{typ}$ and $(V_{TR})_{typ}$ are a little higher than the measured E_{g0} and V_{T0} of about 1.21 V. Though the typical voltages were nearly the same value independent of N4 MOSFET, V_{DD} and T dependence were distinctly improved using N4 n-MOSFET. The improvement by the addition of N4 n-MOSFET is given in Fig. 7. ΔV of ΔV_{BR} and ΔV_{TR} means $\{[V_{min}$ or $V_{max}] - V_{typ}\} \times 100/V_{typ}$ (%), where V_{min} and V_{max} are the minimum and the maximum V under T=−60～+100°C for V_{DD} range of (5.0 ± 1.0) V and (5.0 ± 2.0) V. The average $[(\Delta V_{BR})_{max} - (\Delta V_{BR})_{min}]$ of randomly selected five samples on the same wafer under V_{DD}=5.0± 1.0 (5.0±2.0) V was improved from 3.3 to 1.1 % (from 7.2 to 1.9 %) by adding N4 n-MOSFET

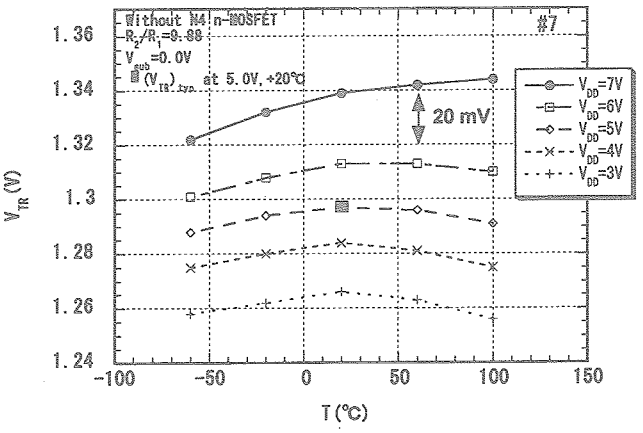


(a)

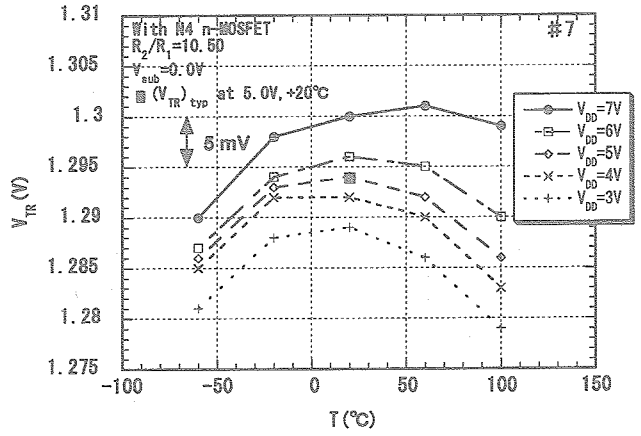


(b)

Fig. 5. Temperature dependence of V_{BR} voltage for various V_{DD} (a) without N4 n-MOSFET and (b) with N4 n-MOSFET in the revised circuit given in Fig. 2.



(a)



(b)

Fig. 6. Temperature dependence of V_{TR} voltage for various V_{DD} (a) without N4 n-MOSFET and (b) with N4 n-MOSFET in the revised circuit given in Fig. 2.

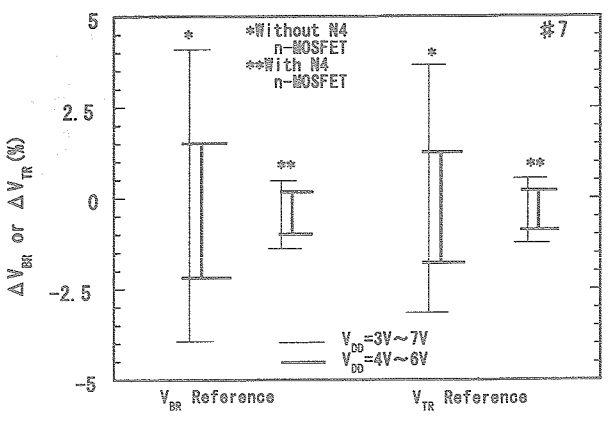


Fig. 7. The change of ΔV_{BR} and ΔV_{TR} due to "without N4 n-MOSFET" and "with N4 n-MOSFET".

to the conventional circuit, while that of ΔV_{TR} was also improved from 2.8 to 1.0 % (from 6.4 to 1.7 %). Consequently, the change of V_{BR} or V_{TR} was improved to about one third using N4 n-MOSFET.

Figure 8 shows (R_2/R_1) ratio dependence of (a) ΔV_{BR} and (b) ΔV_{TR}. To obtain the superior V_{DD} and T stable V_{BR}/V_{TR} characteristics, (R_2/R_1) ratio should be controlled within ±0.1 from the optimum (R_2/R_1) ratio for both cases. The average optimum (R_2/R_1) ratios and its one standard deviations of five samples for V_{BR} and V_{TR} were (12.4 ± 0.2) and (10.3 ± 0.2), respectively. There needs some trimming methods to obtain the optimum (R_2/R_1) ratio for each chip.

ΔV_{BR} and ΔV_{TR} with N4 n-MOSFET for the five samples under the operation condition of V_{DD}=(5.0 ± 1.0)/(5.0 ± 2.0) V and T=−60～+100°C at each optimum (R_2/R_1) ratio are shown in Fig. 9(a) and (b), respectively. The average V_{BR} and V_{TR} were (1.261 ± 0.008) V and (1.288 ± 0.011) V, respectively. The average $[(\Delta V_{BR})_{max} - (\Delta V_{BR})_{min}]$ and $[(\Delta V_{TR})_{max} - (\Delta V_{TR})_{min}]$ were 1.12±0.06 % (1.94±0.09 %) and 1.00±0.04 % (1.75±0.10 %) for V_{DD}=5.0±1.0 V (5.0±2.0 V), respectively. Consequently, V_{TR} reference has a little larger fluctuation of output voltage at the typical condition, but a little smaller V_{DD} and T dependence.

The substrate bias voltage V_{Sub} of both n- and p-MOSFETs were always 0.0 V for the measurements described above. However, V_{TR} voltage can be changed by V_{Sub} supply to n-MOSFETs , because V_{T0} can be varied by V_{Sub} as shown in Figure 10(a), which gives V_{T0} change due to V_{Sub} at I_S=1 μA. V_{T0} changes from 1.21 to 1.63 V dependent on V_{Sub} from 0.0 to

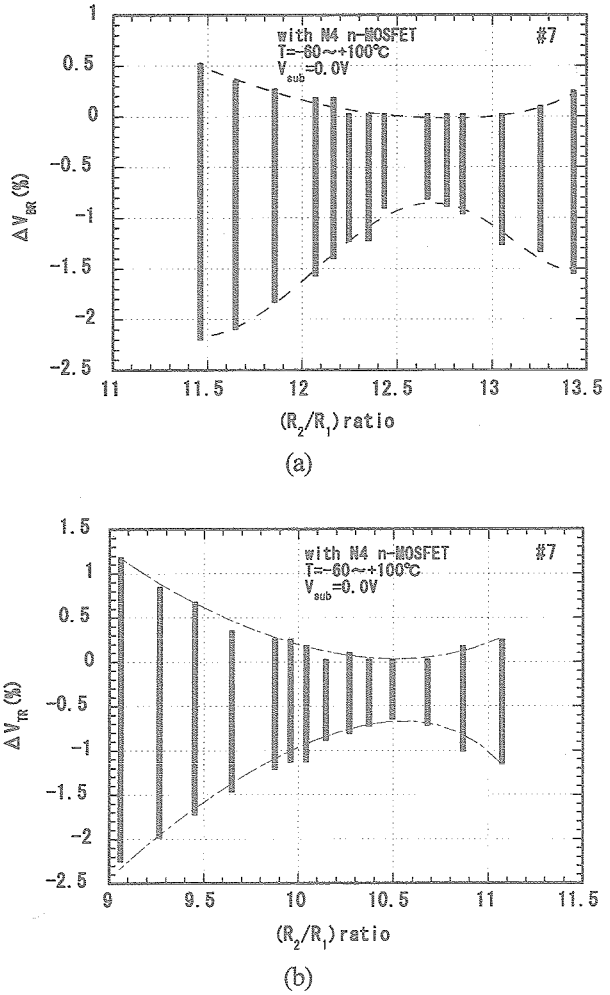


Fig. 8. (R_2/R_1) ratio dependence of (a) ΔV_{BR} and (b) ΔV_{TR}. V_{DD}=5.0 V and T=-60～+100°C.

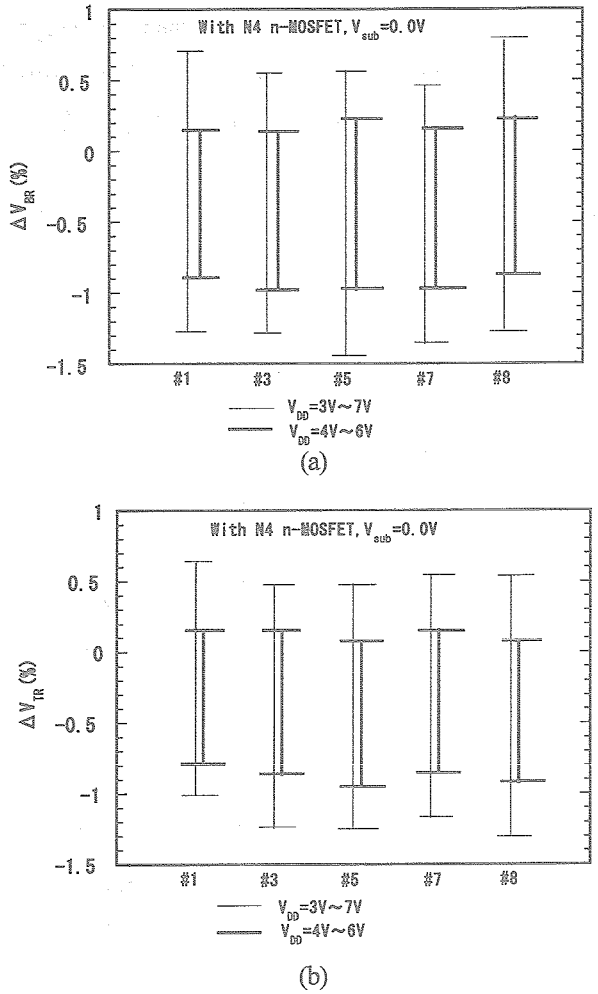
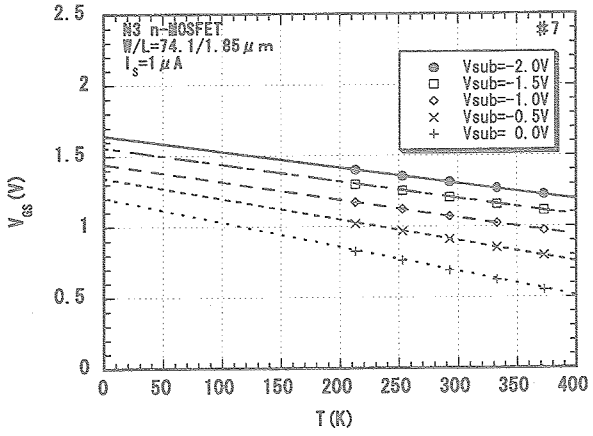


Fig. 9. ΔV_{BR} and ΔV_{TR} variation for five samples on the same wafer under the operation condition of V_{DD}= (5.0 ± 1.0)/(5.0 ± 2.0) V and T=−60～+100°C.

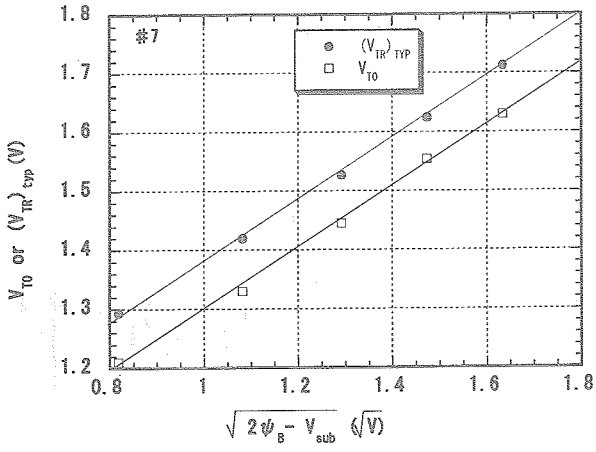
–2.0 V. Figure 10(b) shows $V_{T0}/(V_{TR})_{typ}$ versus $\sqrt{2\psi_B - V_{sub}}$ characteristics, where Ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level and given by $(kT/q)ln(N_A/n_i)$ [19], where N_A and n_i are the substrate carrier concentration and the intrinsic carrier concentration, respectively. $2\Psi_B$ =0.67 V was selected to achieve a linear relation between ΔV_{T0} versus $\sqrt{2\psi_B - V_{sub}}$ characteristics, whereΔV_{T0} means V_{Sub} dependent V_{T0} change from that at V_{Sub}=0.0 V. The $2\Psi_B$ value corresponds to N_A of about 5×10^{15} cm^{-3}, which may be reasonable to the n-well process. The substrate voltage of p-MOSFETs was not supplied in this experiment. $(V_{TR})_{typ}$ changes from 1.29 to 1.71 V in the relation of $(V_{TR})_{typ}=(V_{T0}+0.08)$ V dependent on V_{Sub} from 0.0 to –2.0 V. Figure 10(c) gives ΔV_{TR} versus $\sqrt{2\psi_B - V_{sub}}$ characteristics. Though the optimum (R_2/R_1) ratio changed from 10.2 to 6.9 as V_{Sub} voltage increased from 0.0 to –2.0 V, change of ΔV_{TR} for V_{DD}=5.0 ± 1.0 V and T=–60 ~ +100°C was further improved from 1.0 to 0.6 % by V_{Sub} supply. Change of ΔV_{TR} for V_{DD}=5.0 ± 2.0 V ranged about (1.6 ~ 1.9) % independent of V_{Sub} bias, however, had a tendency to become a little larger under high V_{Sub} supply, because the threshold voltage of n-MOSFETs became so high to degrade V_{DD} dependence of V_{TR} in low V_{DD} region.

4. Conclusion

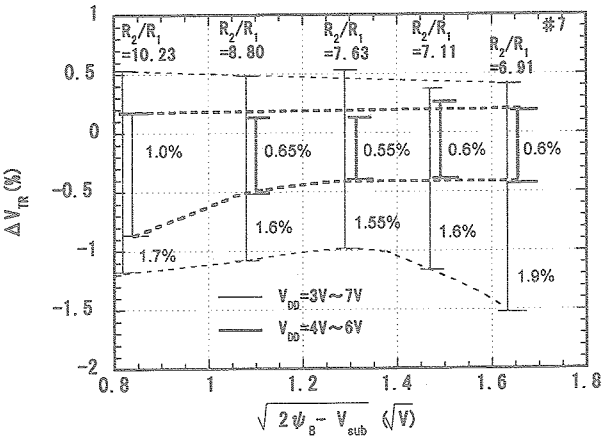
A voltage- and temperature-stable threshold-voltage reference (V_{TR}) circuit with n-MOSFETs biased in subthreshold current region has been presented and compared with a bandgap-voltage reference (V_{BR}). A cascode n-MOSFET device improves the supply voltage and temperature dependence of (V_{BR} /V_{TR}) by suppressing the difference of I-V characteristics, which can not be ignored even in subthreshold region. MOSFET threshold voltage as reference source makes it possible to control output voltage V_{TR} by substrate bias. The circuits were fabricated by 1.2 μm n-well CMOS process. V_{BR}≈1.26 V and V_{TR}≈1.29 V were obtained for both conventional and improved circuits, and were nearly equal to the theoretical values of E_{g0}≈1.21 V (the bandgap at



(a)



(b)



(c)

Fig. 10. (a) V_{GS} versus T characteristics at I_S=1 μA. (b) Change of $V_{T0}/(V_{TR})_{typ}$ and (c) ΔV_{TR} due to the substrate bias voltage V_{Sub} for n-MOSFETs, while the substrate voltage for p-MOSFETs was not supplied. The horizontal axis of (b)/(c) is, while $2\Psi_B$ =0.67 V.

0 K) and V_{T0}≈1.21 V (the threshold voltage at 0 K), respectively. The change of (V_{BR}/V_{TR}) for the supply voltage V_{DD}=5.0±1.0 V and T=−60～+100°C was improved from (3.3/2.8) to (1.1/1.0) %, and its average change of randomly selected five samples fabricated on the same wafer was obtained about (1.12/1.00) % for the revised circuit. V_{TR} reference has a little larger fluctuation of output voltage at V_{DD}=5.0 V and T=+20°C, but a little smaller V_{DD} and T dependence. The controllability of V_{TR} dependent on the substrate bias voltage V_{Sub} supplied to n-MOSFETs was demonstrated. V_{TR} changed from 1.29 to 1.71 V by V_{Sub} supply from 0.0 to −2.0 V, and V_{TR} as well as V_{T0} changed almost linearly to $\sqrt{2\psi_B - V_{sub}}$, where $2\Psi_B$ =0.67 V in the experiments. Change of ΔV_{TR} for V_{DD}=5.0±1.0 V and T=−60～+100°C was further improved from 1.0 to 0.6 % by V_{Sub} supply. The transient stability of V_{BR}/V_{TR} circuits were nearly the same characteristics and the stabilized voltage can be obtained in less than 1 ms for the supply voltage range from 7.0 to 3.0 V.

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電源電圧および温度に対し安定な基準電圧発生回路

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MOSトランジスタのしきい値電圧を用いた基準電圧発生回路(V_{TR})を提案した。サブ・スレッショールド電流領域の特性を利用し、従来のバンドギャップ型の基準電圧回路(V_{BR})よりも、電源電圧(V_{DD})および温度(T)依存性を改善している。また、基板バイアス(V_{Sub})によってしきい値電圧を変化させることができるため、基準電圧出力も制御可能である。ドレイン電圧の不均衡に起因するサブ・スレッショールド電流の差を抑制するため、電圧補償用のn-MOSトランジスタを追加し、V_{DD}および温度依存性を改善した。提案した回路を1.2 μm CMOSプロセスで試作した結果、V_{BR}=1.26 VおよびV_{TR}=1.29 Vの定電圧が得られた。V_{DD} = 5.0 ± 1.0 V、T = −60 ℃～+100℃の範囲での出力(V_{BR}/V_{TR})の変動幅は、電圧補償用トランジスタによって、それぞれ、(3.3/2.8) %から(1.1/1.0) %へ減少できた。出力V_{TR}はV_{BR}に比べて、V_{DD} = 5.0 V、T= + 20℃でのバラツキはやや大きいが、V_{DD}および温度依存性は改善された。V_{Sub}を0から−2.0 Vに変えると、V_{TR}を1.29から1.71 Vへ変化させることができ、V_{DD} = 5.0 ± 1.0 V、T = − 60℃～+100℃でのV_{TR}の変動幅を、1.0から0.6 %へ抑制することができた。

キーワード：バンドギャップ基準電圧，しきい値電圧基準電圧、CMOS

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